

Index

a

Acceleration, 280
 Accelerator, 205
 Adaptive filter, 29
 adaptive beamforming, 30
 algorithms, 30
 applications, 30
 LMS, 31
 LS weights, 33
 RLS, 32
 tap weight, 32
 Adder, 102, 106
 1-bit, 47, 48
 carry-save, 53
 comparison, 51
 n-bit, 49
 SBNR, 56
 ALM, 100
 Altera
 adaptive logic module, 99
 DSP block, 101, 102
 HyperFlex, 103
 M20K, 100
 memory, 100
 MLAB, 100
 Stratix 10, 103
 Stratix V, 98
 Analogue filter networks, 26
 AND matrix, 95
 Antennae, 226

Applications

beamformer, 225
 digital receiver, 314
 fixed beamformer, 216
 lattice filter, 169
 motion estimation, 219
 security, 275
 Architectural synthesis, 204
 Architecture
 choice, 254
 generic, 246
 Manhattan, 97
 Arithmetic
 binary coded decimal, 44
 CORDIC, 58
 fixed-point, 45
 floating-point, 66
 logarithmic number systems, 56
 one's complement, 43
 residue number systems, 57
 signed digit number representation, 55
 signed magnitude, 43
 two's complement, 44
 Arithmetic requirements, 76
 ARM, 107
 Array mapping, 235
 linear, 243
 rectangular, 244
 sparse linear, 244
 sparse rectangular, 245

b

Bayesian classifiers, 278
 Beamformer, 206, 225, 269
 adaptive, 226
 specifications, 229
 Big data, 273
 Black–Scholes, 282
 Block processing, 209
 Block RAM, 122, 219

c

C6000 DSP, 86
 CAL, 148
 Catapult, 147
 CIF, 219
 Circuit architecture, 231
 Classification, 277
 CLB, 105
 Clock, 4, 103
 Clock networks, 103
 Clock tree isolation, 302
 Clustering, 279
 CMOS inverter, 298
 Complex multiplier, 121
 Computational complexity, 74
 Consistency, 202
 Control circuitry, 256
 Controller, 125
 CPU, 72
 DSP microprocessors, 82
 Epiphany, 80
 TMS320C667, 85
 CUDA, 87
 Current block, 122, 219
 Custom circuit, 200
 Cut-set theorem, 163

d

DA, 130
 Data
 independence, 75
 inference, 276
 value, 275
 variety, 274
 velocity, 274
 veracity, 275
 volume, 274

Data analytics, 275
 Data bus, 82
 Data mapping, 313
 Data mining, 277
 Data reordering, 305
 Dataflow, 201
 cyclo-static dataflow, 201
 dataflow process networks, 201
 firing, 201
 homogeneous, 202
 multi-rate, 202
 multidimensional, 201
 multidimensional arrayed, 207
 single-rate, 202
 synchronous dataflow, 201
 Dataflow accelerator, 209
 DCT, 134
 Delay scaling, 163
 Dennard's law, 71
 Dependence graph, 232
 Design
 flow, 9
 languages, 8
 Design choices, 228
 Design reuse, 138
 DFG, 158
 Digital receiver, 206, 314
 Digitization, 12
 Discrete cosine transform, 134
 Discrete Fourier transform, 16
 Discrete wavelet transform, 19
 Distributed arithmetic, 130
 Distributed RAM, 212, 218
 Division
 approximation, 63
 DRx, 206
 DSP
 fixed-coefficient, 126
 interleaving, 156
 parallelism, 156
 pipelining, 156, 160
 processing elements, 120
 recursive filters, 155
 DSP characteristics, 74, 153
 DSP description
 DFG, 158
 SFG, 158

- DSP microprocessor
TMS32010, 82
TMS320C667, 85
- DSP microprocessors, 82
- DSP system, 12
cuts, 161
examples, 13
sampling rate, 14
- DSP transformations, 16
- DSP transforms, 127
- Dynamic voltage scaling, 303
- e**
- Edge, 201
- Epiphany, 80, 81
- eSDK, 80
- Euclidean distance, 285
- f**
- Fast Fourier transform, 17, 314
- FDE, 218
- Field programmable gate array, 2, 94
- FIFO, 202
- Filter, 20
finite impulse response, 20
infinite impulse response, 24
WDF, 25
- Finance
Black–Scholes, 282
Heston, 282
- Finite state machine, 125
- FIR filter, 20, 75, 126, 309
fixed-coefficient, 126
retimed, 162
- Floating-point, 66
- Folding, 174
- FPGA, 2, 94
bandwidth, 113
challenges, 8
data path, 289
DSP block, 106
evolution, 3
mapping, 118, 154, 155
market, 98
memory, 287
processors, 286
programmability, 5
- technologies, 3
tools, 98
Virtex-II Pro, 214
- FPGA acceleration, 281
- FPGA implementation
k-means clustering, 283
Black–Scholes, 282
Heston, 282
- FSM, 125
- FSME, 219
- g**
- GAUT, 148
- Givens rotations
square root free, 36
- GPU, 86
architecture, 87
SMP, 87
- Graphical processing unit, 86
- h**
- HAL, 82
- Hardware abstraction layer, 82
- Harvard, 82
- Heston, 282
- Heterogeneous computing, 4
- High-level synthesis, 140
C-based, 143
CAL, 148
Catapult, 147
GAUT, 148
Impulse-C, 147
LegUp, 150
SDK for OpenCL, 145
Vivado, 143
- i**
- IBM, 281
- iCE40isp, 109
- IIR filter
pipelining, 166
- IIR filters, 24
low-pass, 22
- Impulse-C, 147
- Inductive learning, 276
- Intel, 72
- Interference canceling, 226

Interleaved processing, 209
 Interleaving, 156
 IP cores, 9
 IP design process, 227
 ITRS roadmap, 71

k

k-means clustering
 averaging, 292
 comparison, 292
 distance, 291
 FPGA, 282
 optimizations, 292
 k-slowing, 212
 Karnaugh map, 95

I

Latency, 154
 Lattice filter, 169, 214
 LegUp, 150
 LMS filter, 31
 Locality, 311
 Logarithmic number systems, 56
 Longest path matrix algorithm, 167
 Lookup table, 98, 218
 Low power
 FFT, 311
 LUT, 98, 117
 encoding, 124
 reduction, 123

m

Manhattan distance, 285
 Memory, 121
 Mentor Graphics, 147
 Microsoft, 281
 Catapult, 281
 Mindspeed, 94
 T33xx, 94
 Minimum absolute difference, 219
 Model of computation, 200
 Monolithic Memories, 95
 Moore's law, 1
 Motion estimation, 122, 219
 Multiplier, 102, 106, 308
 Booth's encoding, 54
 carry-save, 53
 Mult18, 216
 Wallace, 54

n

Normalized lattice filter, 214
 Number representations, 42
 binary coded decimal, 44
 one's complement, 43
 signed digit number representation, 55
 signed magnitude, 43
 two's complement, 44
 Nvidia GeForce GPU, 87
 Nyquist rate, 153

o

OpenCL, 87
 OpenCL Details, 146
 Operations
 division, 63
 square root, 60, 64
 OR matrix, 95

p

PAL, 96
 Parallelism, 75
 Parallelella, 80
 Pipelining, 156, 160, 306
 Pipelining period, 167
 PLA, 96
 PLD, 96
 PLL, 103
 Port, 202
 Power consumption, 4, 296
 Altera, 301
 dynamic, 297
 FPGA, 300
 static, 299
 switching activity, 298
 Xilinx, 301
 Printed circuit boards, 1
 Process networks, 201
 dataflow process networks, 201
 Kahn process networks, 201
 Processor, 77
 branches, 289
 flags, 289
 instruction set, 289
 Processors, 286
 Program bus, 82
 Programmability, 6, 72

- Programmable
array logic, 96
logic array, 96
logic devices, 96
- q**
QR array, 233
linear, 256
rectangular, 262
retiming, 250
sparse linear, 258
sparse rectangular, 264
- QR cell
boundary cell, 248
internal cell, 248
- QR-RLS decomposition, 231
- Quine–McCluskey, 95
- r**
Radar, 226
RAM, 121
Rate, 202
RCM
design procedure, 134
- Read-only memory, 96
- Reconfigurable computing, 7
- Reduced coefficient multiplier, 133
- Regression, 278
- Residue number systems, 57
- Retiming, 160, 250
algorithm, 161
cut-set theorem, 163
delay scaling, 163
delay transfer, 163
- RLS algorithm
Givens, 36
- RLS filter, 32
- RLS filters, 231
- ROM, 96
implementation, 123
- s**
Sampling rate, 153
Sampling theory, 14
- Scaling, 71
out, 280
up, 280
- Scheduling
deadlock, 202
- folding, 174
repetitions vector, 203
self-loop, 221
unfolding, 173
- SDK for OpenCL, 145
- Search engine, 280
- Search window, 122, 219
- SFG, 158, 200, 233
- Shift register, 118, 218
- Signal flow graph, 200
- Signed digit number representations, 55
- SMP, 87
- Social media intelligence, 275
- Squared Givens rotations, 36
- SRL, 120, 218
- Stratix, 103
- Support vector machine, 278
- SVM, 278
FPGA, 282
- Switched capacitance, 303, 305
- Synthesis tools
GAUT, 149
- Systolic array, 36
triangular, 91
array, 90
linear, 89
- t**
Technology, 70
scaling, 71
- Throughput rate, 153
- Token, 201
- Topology matrix, 202
- Transforms
DFT, 16
DWT, 19
- Triple-oxide transistor, 301
- u**
Unfolding, 173
- v**
Vivado, 143
- Von Neumann, 77
- w**
Wave digital filter, 25
two-port adaptor, 27

- Wavelet transform, 19
White box component, 210
Wiener–Hopf normal equations, 34
Wordlength, 65
- X**
Xilinx
 block RAM, 105
 CLB, 104
 DSP48E2, 106
 memory, 105
- Z**
Zynq, 107
 APU, 108
 ARM, 107
 programmable logic, 107
 programmable system, 107